Design of 14-bit Continuous-time Oversampling ADC

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ABSTRACT

This paper presents a continuous-time (CT) third-order modulator for single-bit as well as tri-level quantizer. Both topologies cascade of integrator of multiple feedforward (CIFF) as well as cascade of integrator with multiple feedback (CIFB) investigated for better performance. The signal-transfer-function (STF) shows low pass response due to low pass delta-sigma modulator. The noise transfer function (NTF) of the modulator exploited for better noise shaping with NTF zero optimization. The modulator can achieve signal-to-noise ratio (SNR) of 87 dB for single-bit quantizer, while for 1.5-bit quantizer, modulator can achieve SNR of 90 dB with NTF zero optimization with oversampling ratio (OSR) of 64 with full-scale input signal of 400 mV. Due to higher order loop filter much lower out-of-band-gain (OBG) required for higher stability. The operational amplifier is an important building block and needs to be investigated for low power consideration. The proposed modulator is investigated for 400 mV supply amplifier. The topology of the operational amplifier with supply voltage of 400 mV is bulk-driven topology. The bulk-driven amplifier has open loop DC gain of 58 dB and phase margin of 62 degree with power consumption of 3.64 nW. Finally, the complete modulator implementation at the circuit level as RC active amplifier also investigated with thermal noise and flicker noise.

Keywords: Bulk-driven amplifier, Analog-to-digital converter (ADC), Digital-to-analog converters (DACs), NTF, STF.

1. INTRODUCTION

A CT third-order modulator for single-bit as well as tri-level quantizer. Both topologies CIFF as well as CIFB investigated for better performance. The STF shows low pass response due to low pass Delta-Sigma modulator. The NTF of the modulator exploited for better noise shaping with NTF zero optimization. The modulator can achieve SNR of 87 dB for 1-bit quantizer, while for 1.5-bit quantizer, modulator can achieve SNR of 90 dB with NTF zero optimization with OSR of 64 with full-scale input signal of 400 mV. The modulator circuit non-idealities like DC gain, noise from each stage, modeled and simulated. Because of the oversampling ratio required, the bandwidth of a Delta-Sigma modulator (DSM) is restricted by the clock rate. As the nanoscale CMOS techniques are fast evolving, it is now possible to design continuous-time Delta-Sigma modulators with large bandwidth and high dynamic range for high-frequency applications. This work presents a single-loop feedforward third-order 4-bit CTDSM. At a clock rate of 2.4 GHz, this modulator is developed in a 40-nm CMOS process and achieves an 80-dB dynamic range and a 100-MHz bandwidth. From a 1.2 V power source, the modulator uses 69.7 mW [1]. Low oversampling ratios must be used in wideband Delta-Sigma A/D converters in order for the sampling frequency to stay acceptable. For obtaining high resolutions, increase the bit-number or loop order. Cascaded structures are commonly used because high order single-loop modulators are

prone to instability. In the first loop, we utilize a third order modulator rather than a second order modulator to reduce the mismatch sensitivity inherent in cascaded structures. With an OSR of just 8, the suggested 3(5-bit),2(2-bit) cascaded modulator achieves an effective resolution of 14-bits across a bandwidth of 12.5MHz while accounting for all non-idealities. The optimal fifth-order NTF, which contains two pairs of complex conjugate zeros and one dc-zero, maximizes the Signal-to-Quantization-Noise-Ratio (SQNR). Feed-forward pathways, which add the signal directly at the quantizer input, loosen the integrator parameters, result in low distortion [2]. A fourth-order, multi-stage noise shaped (MASH) DSM for broad bandwidth applications is presented in this work. A second order DSM with multi-level quantizer is used in each stage of the DSM. The first stage of the DSM is a low-distortion second-order single-loop DSM, and the second stage is a low-distortion DSM with Chebyshev type II filtering. The proposed design can increase circuit performance by reducing signal distortion. The TSMC 0.25 m process was used to develop and construct a test DSM chip for ADSL applications. The simulation results show that with 65mW of power dissipation, the dynamic range (DR) might approach 87dB [3]. For 20-MHz signal bandwidth (BW) a high degree of linearity multi-stage noise Shaping (MASH) 2–2–2 DSM was described. Multi-bit quantizers were used to give a low quantization noise level in each stage. As a result, the modulator's SNR will be improved. A multi-layer butterfly-type network-based randomization strategy was created to reduce spurious tones in the output spectrum, and mismatch noise in internal multi-bit DACs was explored in depth. At a sample rate of 320MHz, the modulator took up 0.45mm of chip area and dissipated 28.8mW from a 1.8-V power supply, thanks to its fabrication in a 0.18-m single-poly 4-metal Complementary Metal Oxide Semiconductor (CMOS) process. The measured spurious-free dynamic range (SFDR) was 94dB, with the randomizers for multi-bit DACs providing a 17-dB increase in the first two stages. The figure-of-merit (FOM) was 126pJ/conv, and peak signal-to-noise and distortion ratio (SNDR) was 76.9dB at 1 dBFS @ 2.5-MHz input [4].

This paper presents a continuous-time third-order modulator for single-bit as well as tri-level quantizer. Both topologies CIFF as well as CIFB investigated for better performance. The STF shows low pass response due to low pass delta-sigma modulator. The NTF of modulator exploited for better noise shaping with NTF zero optimization. The modulator can reach SNR of 87 dB for single-bit quantizer, while for 1.5-bit quantizer, modulator can reach SNR of 90 dB with NTF zero optimization with OSR of 64 with full-scale input signal of 400 mV. Due to higher order loop filter much lower OBG required for higher stability. The operational amplifier is an important building block and needs to be investigated for low power consideration. The proposed modulator is investigated for 400 mV supply amplifier. The topology of the operational amplifier with supply voltage of 400 mV is bulk-driven topology. The bulk-driven amplifier has open loop DC gain of 58 dB and phase margin of 62 degree with power consumption of 3.64 nW. Finally, the complete modulator implementation at the circuit level as RC

active amplifier also investigated with thermal noise and flicker noise.

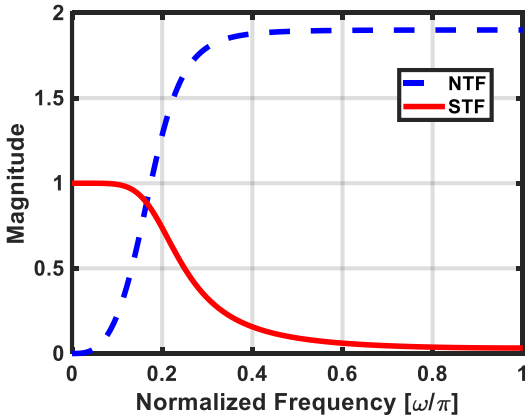

Figure 1: STF and NTF plot (CIFB)

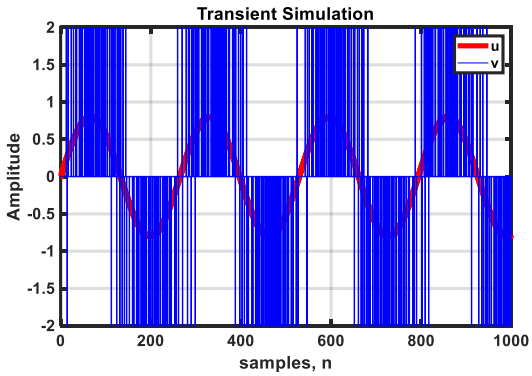

Figure 2: STF and NTF plot (CIFB)

After the introduction, the second section discuss the design of the modulator design with CIFB topology, while the third section

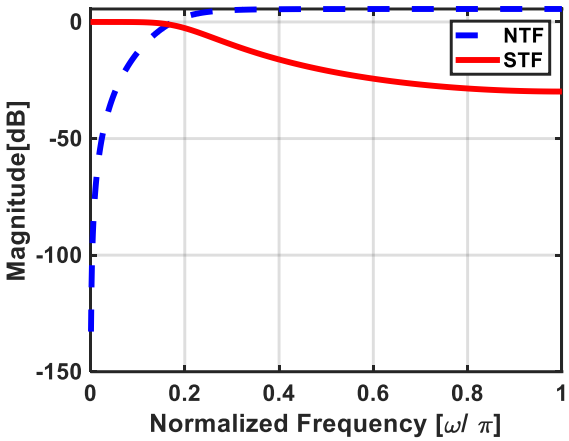

Figure 3: STF and NTF plot (CIFB)

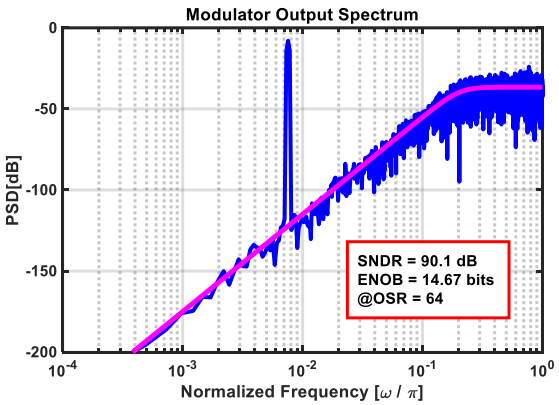

Figure 4: Output PSD plot (CIFB)

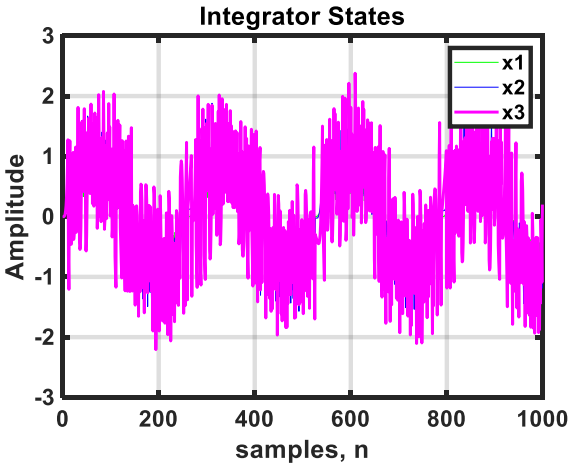

Figure 5: Output states of the integrators

describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the third-order single-bit & tri-level quantizer for CT design implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

A higher order with three integrators in the loopfilter and five-bit quantizer modulator modeled using Delta-Sigma Toolbox [12]. The CIFB investigate for higher OBG with low oversampling ratio of 64 without NTF zero optimization technique. The modulator with CIFB topology can achieve SNR of 90 dB with OSR of 64. Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The coefficients of the proposed third order with 5-bit quantizer CIFB obtained from Delta-Sigma Toolbox. These coefficients represent the ratio of capacitors at the discrete-time implementation of the modulator. While for the CT implementation these coefficient needs to be converted into the CT equivalent coefficient [13]. Then these converted coefficients will be used to choose the resistor and capacitor ratio considering the sampling frequency. Those coefficients which are not mentioned, have value zero. The STF and NTF of the modulator is shown in Figure 1. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is less than 2 for high stability of the modulator. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The Figure 2 shows the transient output of the modulator with pulse coded modulation (PCM). The Figure 3 shows that STF and NTF plot, as the NTF shows -60dB/decade for the quantization noise attenuation due to three integrators inside the loop filter. The maximum quantization attenuated as all the integrators are ideal. The Figure 4 shows the output power spectral density (PSD) plot with SNR of 68, achieving effective number of bit (ENOB) of 14-bit. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loopfilter is assumed having infinite DC gain. The noise floor is at the level of -130dB, the quantization noise is suppressed maximum with three integrators inside the loop filter. Due to low OSR of 64, the signal bandwidth is small. Due to CIFB topology of the modulator the signal swing inside the loopfilter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Due to CIFB topology the stability of the loopfilter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loopfilter. The Figure 5 shows the output states of the modulator, due to CIFB topology the swing inside the loopfilter is large.

3. RESULTS & DICUSSION

A third-order single-bit modulator for wideband applications is proposed. The topology of the modulator is CIFB to lower the power of the loopfilter. The modulator can achieve SNR of 90 dB with OSR of 64. The simulation environment Delta-Sigma Toolbox [14] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A continuous-time third-order modulator for single-bit as well as tri-level quantizer. Both topologies CIFF as well as CIFB investigated for better performance. The STF shows low pass response due to low pass DSM. The NTF of the modulator exploited for better noise shaping with NTF zero optimization. The modulator can achieve SNR of 87 dB for single-bit quantizer, while for 1.5-bit quantizer, modulator can achieve SNR of 90 dB with NTF zero optimization with OSR of 64 with full-scale input signal of 400 mV. Due to higher order loop filter much lower out-of-band-gain OBG required for higher stability. The operational amplifier is an important building block and needs to be investigated for low power consideration. The proposed modulator is investigated for 400 mV supply amplifier. The topology of the operational amplifier with supply voltage of 400 mV is bulk-driven topology. The bulk-driven amplifier has open loop DC gain of 58 dB and phase margin of 62 degree with power consumption of 3.64 nW. Finally, the complete modulator implementation at the circuit level as RC active amplifier also investigated with thermal noise and flicker noise.

5. ACKNOWLEDGMENT

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6. REFERENCES

[1] **Y. Xiao, et al, 2020,** A 100-MHz Bandwidth 80-dB Dynamic Range Continuous-Time Delta-Sigma Modulator with a 2.4-GHz Clock Rate, Nanoscale Research Letters, 58(15).

[2] **E. . Di,. Gioia et al, 2006,** A 14-bit cascaded 32-2 Sigma-Delta Modulator for VDSL, IEEE International Modwest Symposium on Circuit and Systems, July 2007.

[3] **J. Chiang, et al, 2004**, A 2.5-V 14-bit MASH sigma-delta modulator for ADSL, Processing of 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits, November 2004.

[4] **D. Li, et al, 2020**, A 20-MHz BW MASH Sigma-Delta Modulator with Mismatch Noise Randomization for Multi-Bit DACs, Journal of Circuits, Systems and Computers, 29(7), pp.

[5] **A. AMA, et al, 2006,** A 14-bit 125 Ms/s IF/RF sampling pipelined ADC with 100 dB SFDR and 50 fs jitter, IEEE Journal of Solid-State Circuits, 41(8), pp. 1846-1855.

[6] **Bolatkale M, et al,2011,** A 4 GHz continuous-time delta-sigma ADC with 70-dB DR and -74 dBFS THD in 125 MHz BW, IEEE Journal of Solid-State Circuits, 46(12), pp. 2857-2868.

[7] **Caldwell T, et al, 2014,** A reconfigurable Delta-Sigma ADC with up to 100 MHz using flash reference shuffling, IEEE Trans Circuit & Syst-I: Regular paper, 61(8), pp. 2263-2271.

[8] **Srinivasan V, et al, 2012,** A 20 mW 61dB SNDR (60 MHz BW) 1b 3rd-order continuous-time delta-sigma modulator clocked at 6GHz in 45nm CMOS, IEEE International Solid-State Circuit Conference, pp. 158-160.

[9] **Yoon D, et al, 2015,** A continuous-time sturdy-MASH Delta-Sigma Modulator in 28nm CMOS, IEEE Journal of Solid-State Circuit, 50(12), pp. 2880-2890.

[10] **S. Norsworthy, Richard Schreier, G.C. Temes**,1997, Delta-Sigma Data Converter Theory, Design, and Simulation, John Wiley & Sons, Inc., Hoboken, New Jersey.

[11] **Sheng-Jui Huang , et al., 2017,** A 125MHz-BW 71.9dB-SNDR VCO-

Based CT delta-sigma ADC with segmented Phase-Domain ELD Compensation in 16nm, IEEE International Solid-State Circuit Conference (ISSCC), pp. 470-472.

[12] **Yunzhi Dong , et al., 2016,** A 930mW 69db-DR 465MHz-BW CT 1-2 MASH ADC in 28 nm CMOS, IEEE International Solid-State Circuit Conference (ISSCC), pp. 278-280.

[13] **R. Scherier** Delta-Sigma Toolbox ((http://www.mathworks.com/matlancentral/fileexchange/19-delta-sigma-toolbox).

[14] **Shanti Paven, Richjard Schreier and G.C. Temes,** Understanding Delta-Sigma Data Converters Second Edition , IEEE Press Wiley

[15] **S. Brigati** SDToolbox (http://www.mathworks.com/matlabcentral/fileexchange/2460-sd-toolbox).